REMARKS

Claims 1-20 are pending in the application. Claims 1, 6, 11, 14, and 16 are independent. Claims 1, 11, and 16 have been amended. It is believed that these changes introduce no new matter and their entry is respectfully requested.

Objection to the Drawings

In paragraph 3 of the Office Action, the Examiner objected to the drawings stating that the drawings failed to show "A processor, comprising: front end logic to receive a control signal; and configuration logic coupled to the front end logic to inhibit booting up..." as recited in claim 11. By the foregoing Amendment, Applicants have canceled "front end logic" and "configuration signal logic" from claim 11. Such cancellation renders the objection moot. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objection to the drawings.

Claim Objections

In paragraph 4 of the Office Action, the Examiner objected to claim 16 because of informalities. Specifically, the Examiner requires that line 5 be changed from "on" to "one." By the foregoing Amendment, Applicants have amended claim 16 to accommodate the objection. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objection to claim 16.

Rejection of Claims 1-5 Under 35 U.S.C. §112, Second Paragraph

In paragraph 6 of the Office Action, the Examiner rejected claims 1-5 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim that which the Applicants regard as the invention. Specifically, the Examiner states that the language "a proper fuse block voltage" recited in claim 1, line 10, can be interpreted either as (1) a control signal having an appropriate voltage level or (2) that the fuse block is supplied by a voltage that has a proper supply level voltage. By the foregoing Amendment, Applicants have amended claim 1 to recite "a proper supply voltage level." This Amendment accommodates the Examiner's rejection. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claim 1. Claims 2-5 properly depend from claim 1 and thus Applicants respectfully

request that the Examiner reconsider and remove the rejections to claims 2-5.

Rejection of Claims Under 35 U.S.C. §103(a)

In the Office Action, the Examiner rejected claims 1-8 and 14-16 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,951,681 to Chang (hereinafter "Chang") in view of U.S. Patent No. 6,433,405 to Gunderson et al. (hereinafter "Gunderson") and U.S. Patent No. 5,630,090 to Keehn et al. (hereinafter "Keehn"). To establish a *prima facie* case of obviousness, an Examiner must show three things: (1) that there is some suggestion or motivation to modify a reference or combine reference teachings to arrive at the claimed invention, (2) that there must be a reasonable expectation of success, and (3) that the references teach or suggest each and every element of the claimed invention. (MPEP §2143.) The suggestion or motivation to modify reference teachings must be found in the references relied upon (MPEP §2143.01). The proposed modification cannot render the cited reference unsatisfactory for its intended purpose, however, or change the principle of operation. (Id.) Applicants respectfully traverse the rejection.

Chang appears to be directed to a plug and play CPU that allows different CPUs that have different operating frequencies and voltages to be plugged into the same socket and have them work as designed. The problem addressed in Change is that every time a CPU with different operating frequencies and voltages is plugged into a socket, the jumpers for the operating frequencies and voltages have to be changed. The solution proposed is to issue a warning message to a user (i.e., one who plugs a new CPU into a socket) that the operating frequencies and voltages need to be changed. The user then changes the operating frequencies and voltages set in the system firmware (BIOS).

In the Office Action, the Examiner essentially asserts that Chang teaches "a control signal coupled to the processor, the voltage regulator (signal from the voltage controller to the voltage converter), and a control signal coupled to the processor and the clock generator (frequency generator, the clock is controlled by a signal from the frequency controller) to prevent (preventing an incorrect setting of voltage and frequency form destroying the processor) the processor from receiving the processor voltage and the

processor clock until a voltage configuration signal and a frequency configuration signal to specify the processor voltage and the processor clock frequency (new user settings for CPU)" is received. Applicants respectfully disagree with the Examiner's characterization of Chang.

Applicants respectfully submit that Change does not teach a control signal coupled to the processor, the voltage regulator (***signal from the voltage controller*** to the voltage converter), and a control signal coupled to the processor and the clock generator (frequency generator, the clock is controlled by a ***signal from the frequency controller***) to prevent (preventing an incorrect setting of voltage and frequency form destroying the processor) the processor from receiving the processor voltage and the processor clock until a voltage configuration signal and a frequency configuration signal to specify the processor voltage and the processor clock frequency (new user settings for CPU)" as the Examiner asserts. As an example, the signal from the voltage controller to the voltage converter does not prevent the processor from receiving the processor voltage until a voltage configuration signal is received. Additionally, the signal from the frequency controller does not prevent the processor from receiving the processor frequency until a frequency configuration signal is received.

Assuming for the sake of argument, that Chang teaches what the Examiner asserts, however, the Examiner concedes that Chang fails to teach "a single control signal, ...a fuse block programmed [with] the voltage configuration and the frequency configuration to specify the processor voltage and clock frequency, ... [and] wherein the fuse block has a proper voltage." The Examiner cites Gunderson and Keehn to make up for these deficiencies. Applicants respectfully disagree.

As a first matter relating to the single control signal, the Examiner argues that it would have been obvious to modify Chang by integrating both control signals in order to reduce the number of control lines thereby reducing the space required for the invention. Applicants respectfully disagree. In Chang, the ***signal from the voltage controller*** is a voltage and the ***signal from the frequency controller*** is a frequency. Applicants respectfully submit that the combination proposed (i.e., combining the voltage from the

voltage controller with the frequency from the frequency controller) would change the principle of operation of Chang. For example, combining the voltage signal (i.e., the voltage from the voltage controller) with frequency signal (i.e., the frequency from the frequency controller) and applying the resulting signal to the CPU phase latched loop (PLL) of Chang would cause the CPU PLL to operate at the initial voltage (i.e., the output of the voltage controller) rather than the setting voltage or working voltage. This is contrary to the operating principles of Chang and is thus not a proper basis for an obviousness rejection.

As for the fuse block, the Examiner asserts that it would have been obvious to modify the "storage device" in Chang with the fuse block in Gunderson because Gunderson teaches that "his fuse block desirably increases the probability that the programming will be successful." Applicants respectfully disagree.

Gunderson is directed to programming a fuse block with CPU specific operating parameters. This is in direct contrast to Chang, which assumes that the operational parameters are already programmed in the CPU and that the problem is that the programmed operational parameters vary from part to part. Chang is not interested in programming the CPU and such modification would change the intended purpose of Change. Such modification thus is not a proper basis for an obviousness rejection.

The Examiner asserts further that it would have been obvious to modify Chang and Gunderson with Keehn to prevent the processor from accessing the fuse block until the fuse block has a proper voltage because the fuse block is a type of memory and to ensure that correct data was supplied to the processor. Applicants respectfully disagree. Keehn is directed to power-saving circuits. Applicants respectfully submit that combining Keehn with Chang or Gunderson make Chang or Gunderson unsatisfactory for their intended purposes.

Because the Examiner has not made out a *prima facie* case of obviousness with respect to claims 1-20 Applicants respectfully submit that claims 1-20 are patentable over

the cited art. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 1-20.

CONCLUSION

Applicants submit that all grounds for objection and rejection have been properly traversed accommodated, or rendered moot and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 2/17/2004

Jan Little-Washington
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